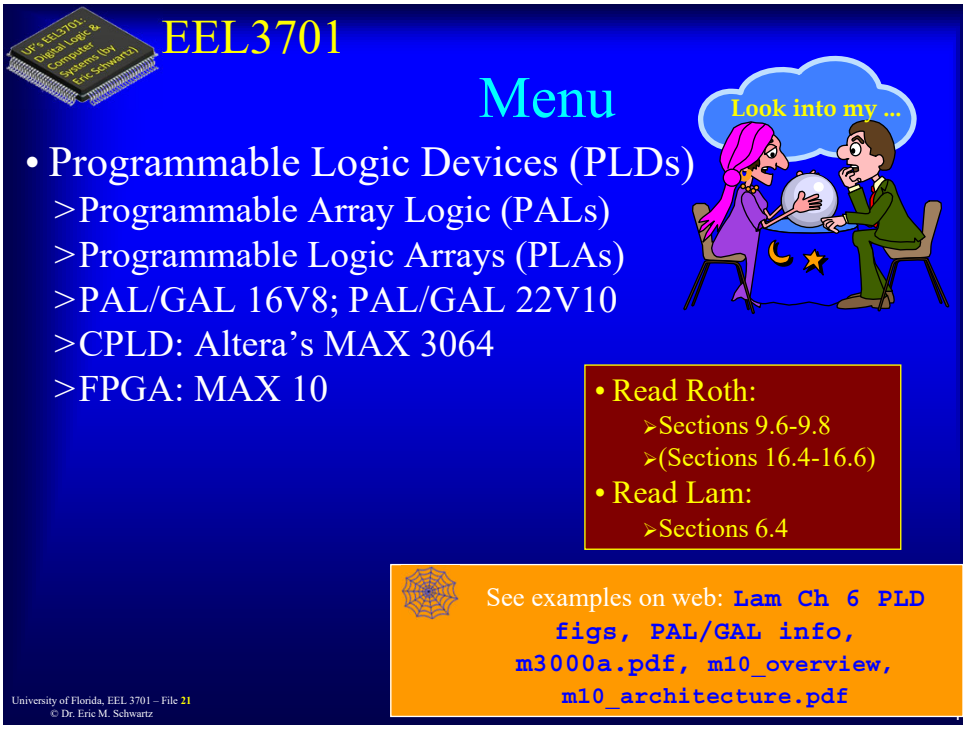
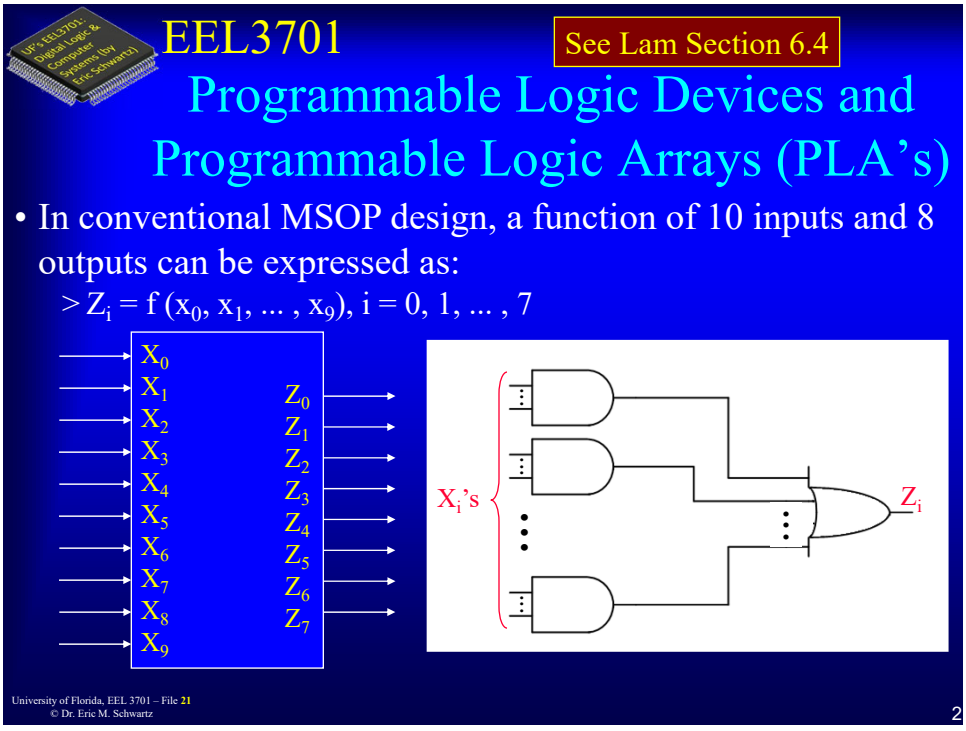
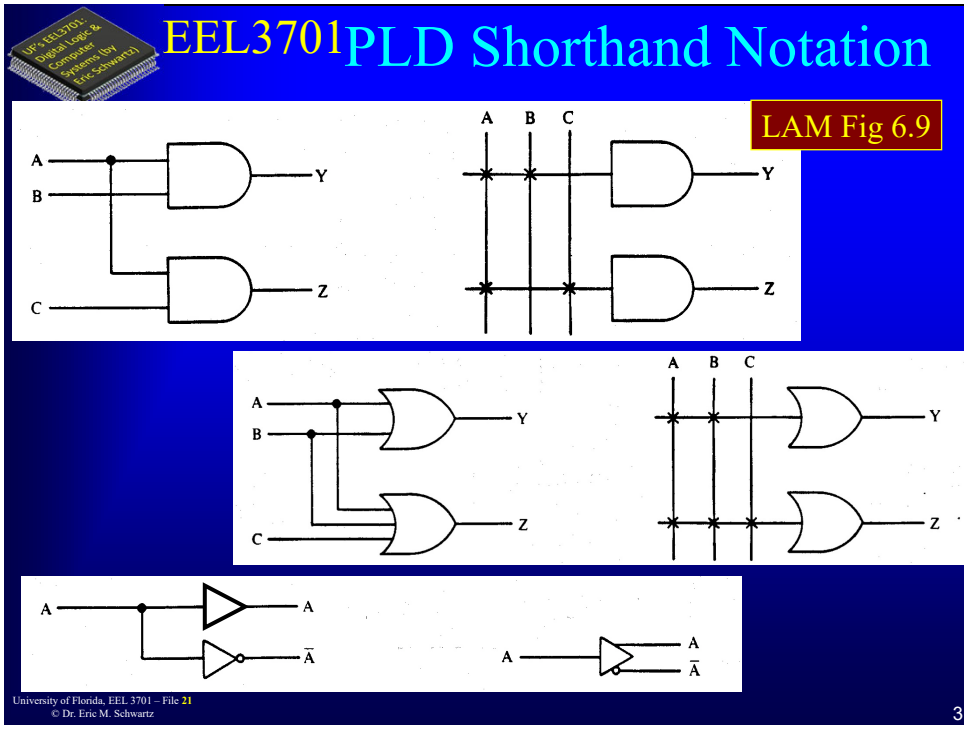

EEL3701
Menu
• Programmable Logic Devices (PLDs)
>Programmable Array Logic (PALs)
>Programmable Logic Arrays (PLAs)
>PAL/GAL 16V8; PAL/GAL 22V10
>CPLD: Altera's MAX 3064
>FPGA: MAX 10
Look into my ...
• Read Roth:
➢Sections 9.6-9.8
➢(Sections 16.4-16.6)
• Read Lam:
➢Sections 6.4
See examples on web: Lam Ch 6 PLD figs, PAL/GAL info, m3000a.pdf, m10_overview, m10_architecture.pdf
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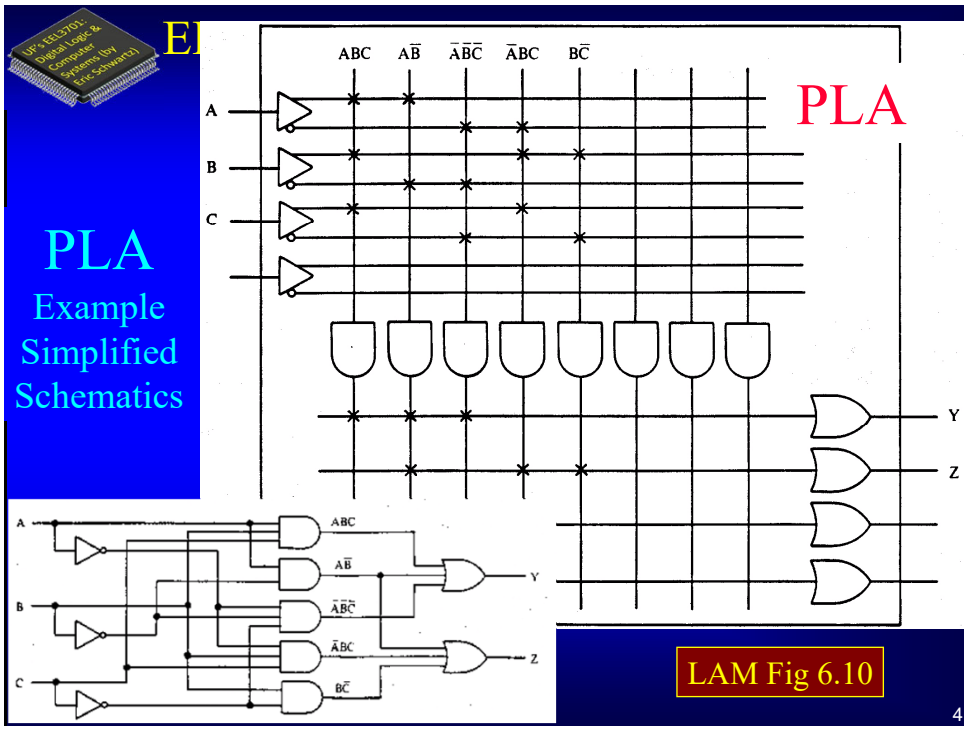
1


EEL3701
See Lam Section 6.4
Programmable Logic Devices and Programmable Logic Arrays (PLA's)
• In conventional MSOP design, a function of 10 inputs and 8 outputs can be expressed as:
> $Z_i = f(x_0, x_1, \ldots, x_9)$, i = 0, 1, ... , 7
$X_0$ $X_1$ $X_2$ $X_3$ $X_4$ $X_5$ $X_6$ $X_7$ $X_8$ $X_9$
$Z_0$ $Z_1$ $Z_2$ $Z_3$ $Z_4$ $Z_5$ $Z_6$ $Z_7$
$X_i$'s
$Z_i$
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2

2

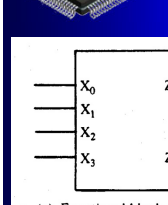

EEL3701
PLD Shorthand Notation
LAM Fig 6.9
A
B
C
Y
Z
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3

3


PLA
Example
Simplified
Schematics
ABC
AB̄
ĀB̄C̄
ĀBC
BC̄
A
B
C
Y
Z
LAM Fig 6.10
4

4

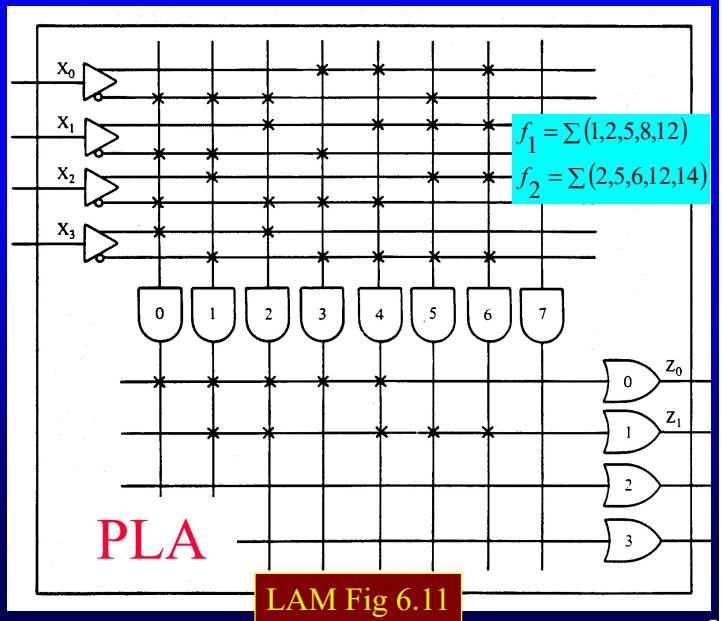
## EEL3701 Simplified Schematics




(a) Functional block diagram

| $X_0$ | $X_1$ | $X_2$ | $X_3$ | $Z_0$ | $Z_1$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

(b) Truth table




LAM Fig 6.11

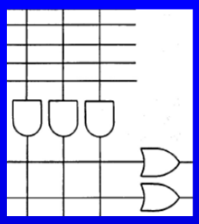


## EEL3701 Programmable Logic Devices and Programmable Logic Arrays (PLA's)

- **Q:** PLA's use SOPs. Any problems with using only SOPs?
  **A:** _____
- **Q:** Why not us POSs? **A:** _____
- PLA's are not a new, but a systematic technique for realizing combinational logic in a single package (IC). This allows us to take advantage of LSI (Large-Scaled Integration).

EEL3701

## PLA Block Diagram



N Inputs → Inv / Non-Inv Buffers → 2*N → AND Array (K AND terms) → K → OR Array → M Outputs

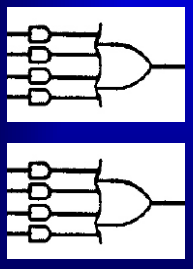
- PLAs OR gates share AND gates, i.e., have access to all the AND gates



7

EEL3701

## PAL Block Diagram

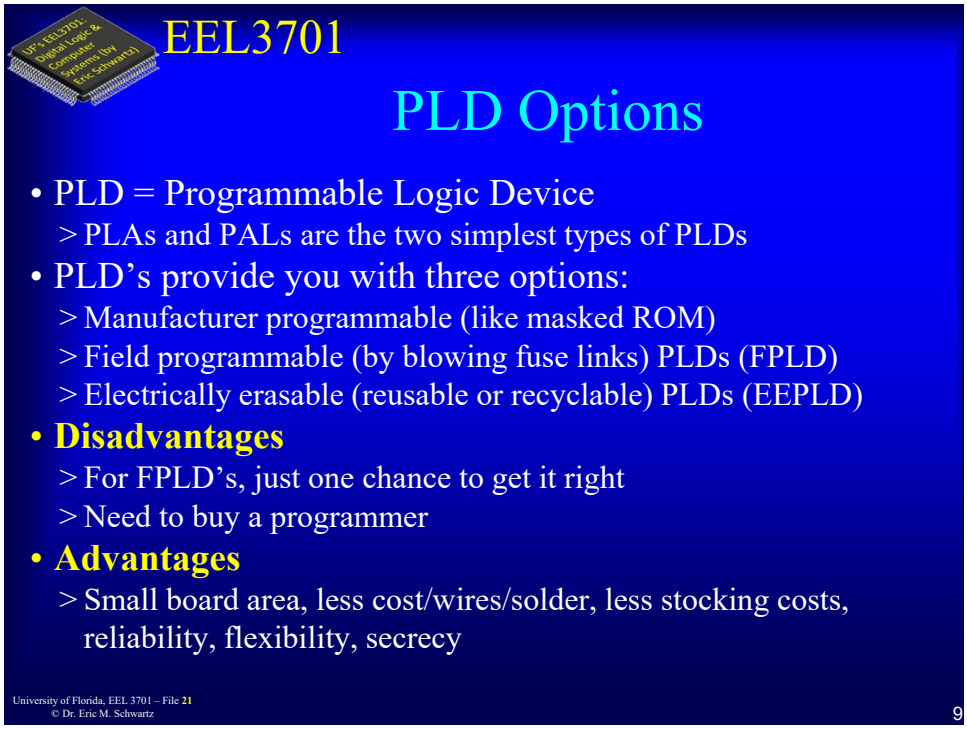


N Inputs → Inv / Non-Inv Buffers → 2*N → AND Array ($K_{M-1}$ terms), AND Array ($K_{M-2}$ terms), AND Array ($K_0$ terms) → $K_{M-1}$, $K_{M-2}$, $K_0$ → OR, OR, OR → $Output_{M-1}$, $Output_{M-2}$, $Output_0$

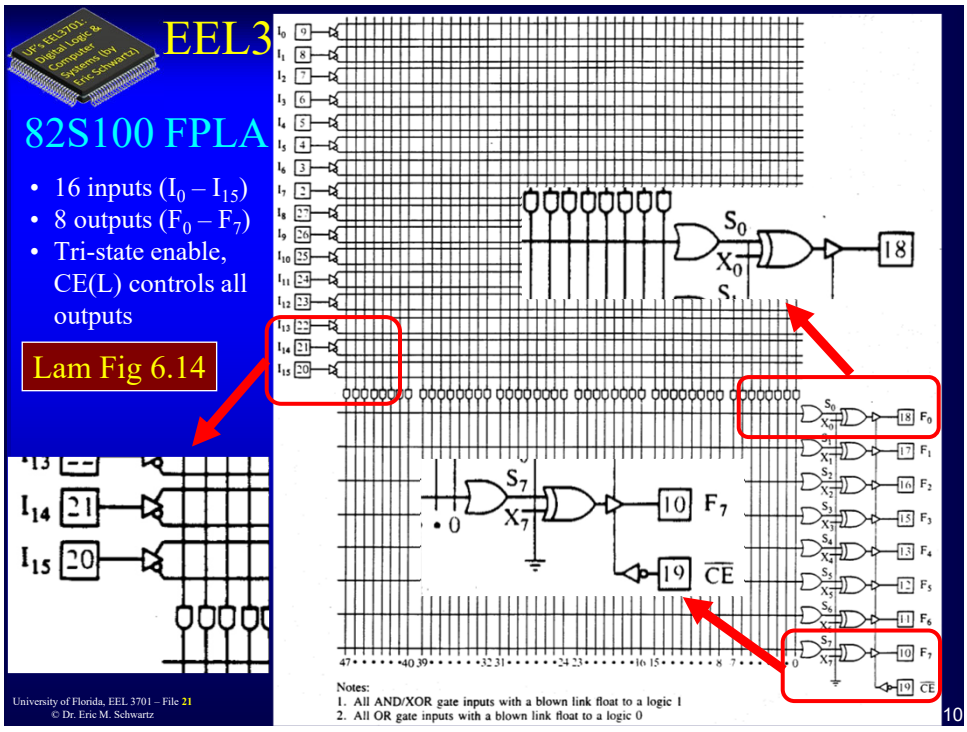
- PALs do **NOT** share AND gates, i.e., each PAL OR gate has its own AND gates



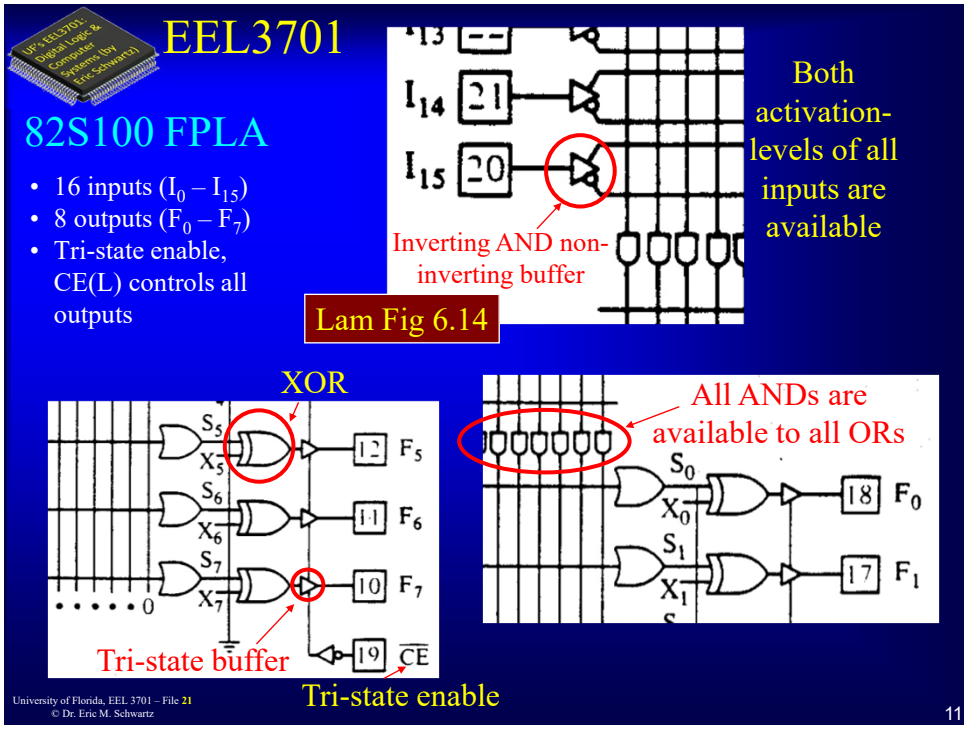
8


EEL3701
PLD Options
• PLD = Programmable Logic Device
> PLAs and PALs are the two simplest types of PLDs
• PLD's provide you with three options:
> Manufacturer programmable (like masked ROM)
> Field programmable (by blowing fuse links) PLDs (FPLD)
> Electrically erasable (reusable or recyclable) PLDs (EEPLD)
• Disadvantages
> For FPLD's, just one chance to get it right
> Need to buy a programmer
• Advantages
> Small board area, less cost/wires/solder, less stocking costs, reliability, flexibility, secrecy
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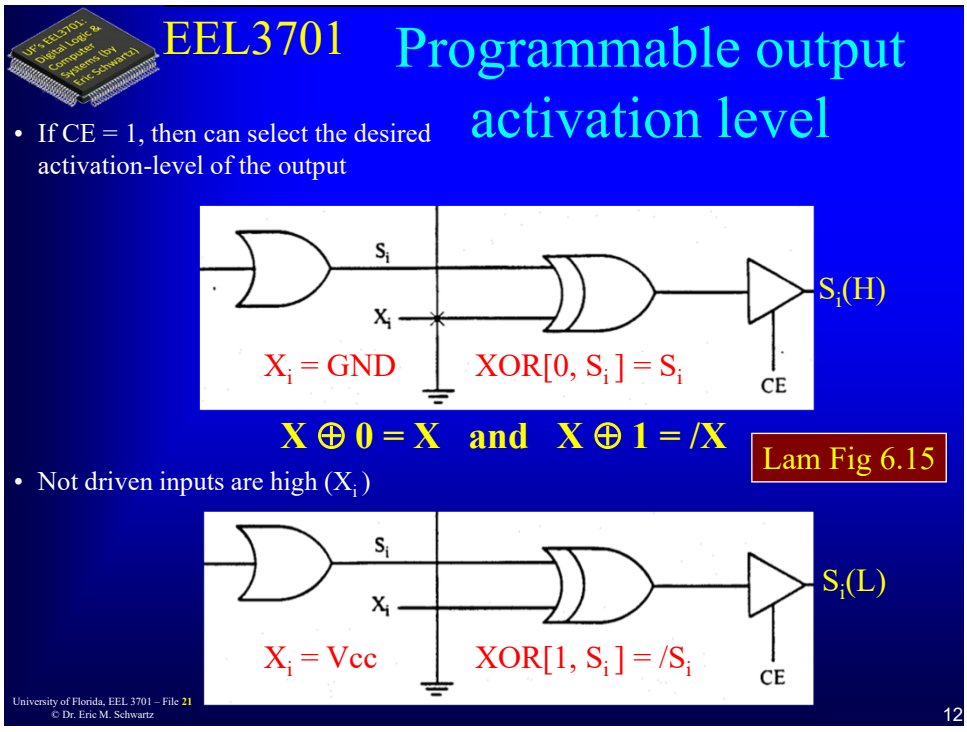
9


EEL3
82S100 FPLA
• 16 inputs ($I_0 – I_{15}$)
• 8 outputs ($F_0 – F_7$)
• Tri-state enable, CE(L) controls all outputs
Lam Fig 6.14
$I_{14}$ 21
$I_{15}$ 20
$S_0$
$X_0$
18
$S_7$
$X_7$
10 $F_7$
19 $\overline{CE}$
Notes:
1. All AND/XOR gate inputs with a blown link float to a logic 1
2. All OR gate inputs with a blown link float to a logic 0
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10


EEL3701
82S100 FPLA
• 16 inputs ($I_0 - I_{15}$)
• 8 outputs ($F_0 - F_7$)
• Tri-state enable, CE(L) controls all outputs
Lam Fig 6.14
Inverting AND non-inverting buffer
Both activation-levels of all inputs are available
XOR
All ANDs are available to all ORs
Tri-state buffer
Tri-state enable
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11


EEL3701
Programmable output activation level
• If CE = 1, then can select the desired activation-level of the output
$X_i$ = GND
XOR[0, $S_i$] = $S_i$
$S_i$(H)
X ⊕ 0 = X and X ⊕ 1 = /X
Lam Fig 6.15
• Not driven inputs are high ($X_i$)
$X_i$ = Vcc
XOR[1, $S_i$] = /$S_i$
$S_i$(L)
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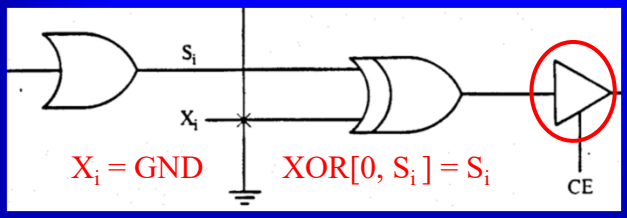
12

EEL3701

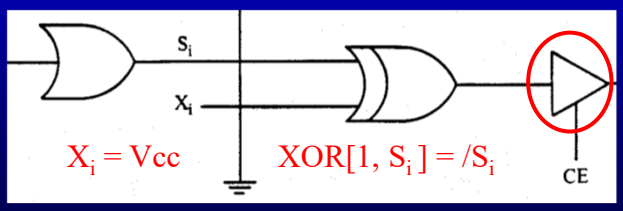
# Tri-state outputs

Lam Fig 6.15

- If CE = 0, then output is tri-stated
- If CE = 1, then output is not tri-stated




$S_i$(H), if CE=1
Hi-Z, if CE=0




$S_i$(L), if CE=1
Hi-Z, if CE=0



EEL3701

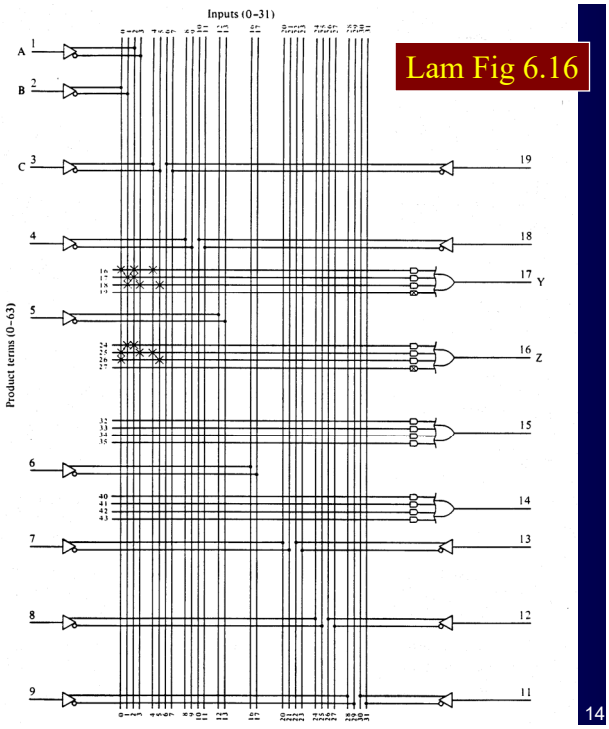
# PAL14H4

- PALs do **NOT** share, i.e., they have their own ANDs
- 14 inputs
- 4 ANDs per OR
- 4 outputs (ORs)

Y = ABC + A /B + /A /B /C

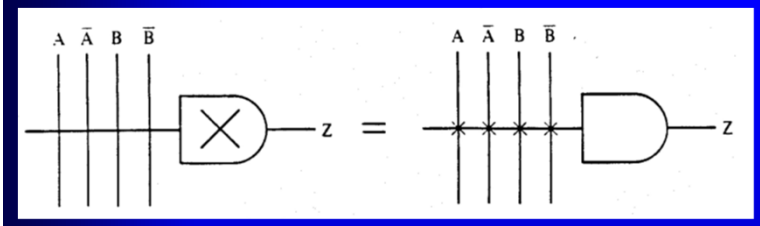
Z = A /B + /A B C + B /C

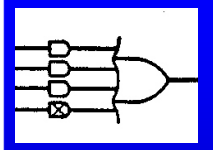
Lam Fig 6.16



EEL3701

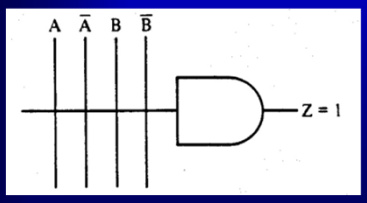
## PAL Abbreviations

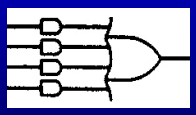


The X in the AND ➔ all inputs connected, i.e., Z = A*/A*B*/B = 0
➔ AND gate is not used

Lam Fig 6.17



Nothing in AND or connected to AND ➔ no inputs connected, i.e., Z = 1
So what is the output of this OR gate? ___

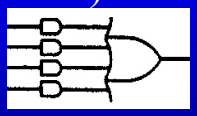


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EEL3701

## Programmable Array Logic (PAL)

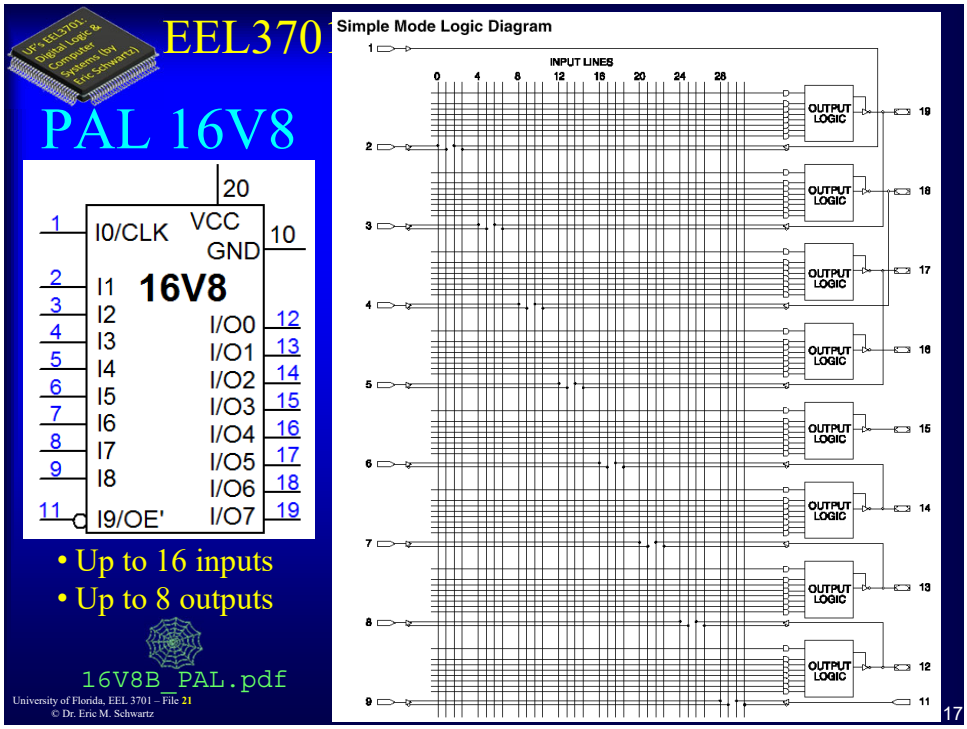
- PAL is a special case of PLAs
- PALs have a **fixed** OR array (instead of the programmable OR Array for the PLA), i.e., PALs do **NOT** share (each OR needs its own ANDs)



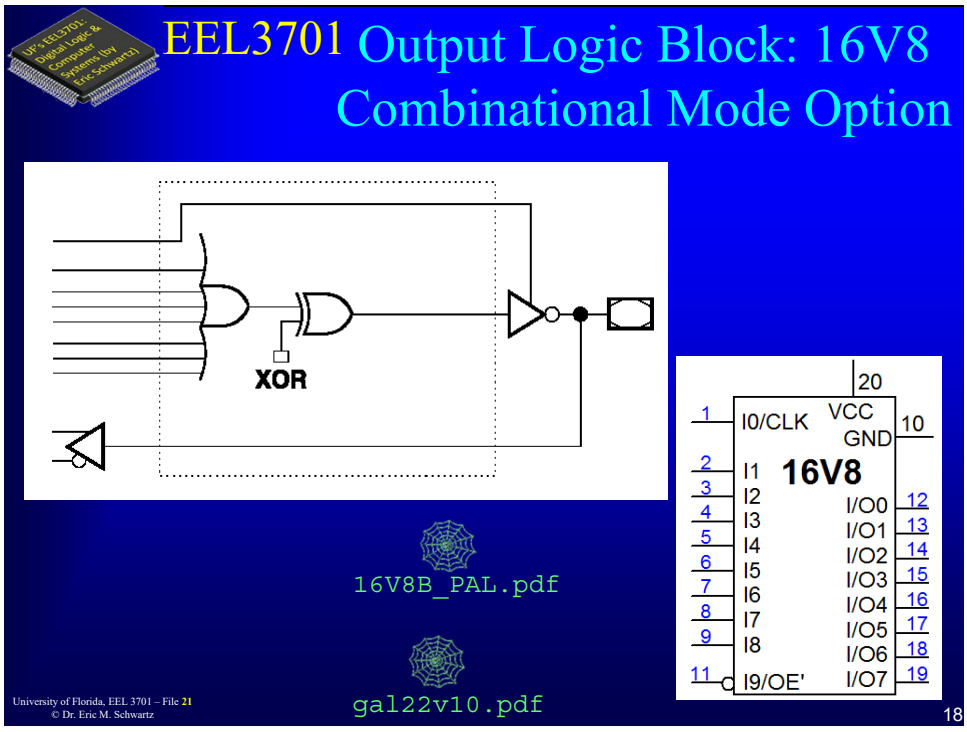
- PALs are cheaper than PLA, but less flexible



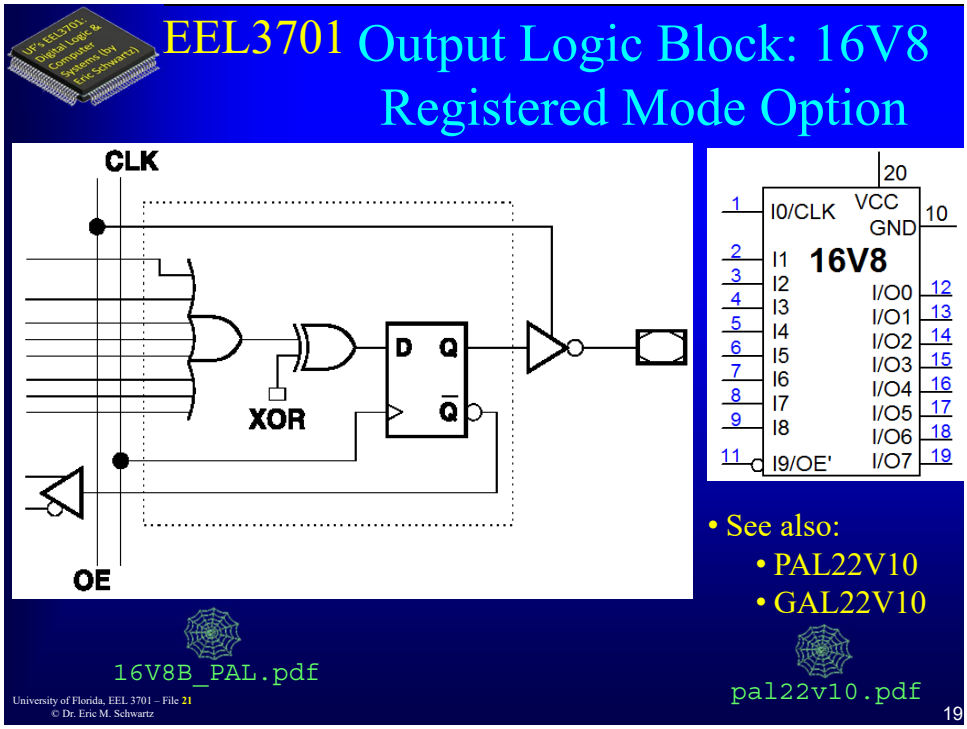
16


EEL3701
PAL 16V8
20
I0/CLK
VCC
GND
10
I1
16V8
I2
I3
I4
I5
I6
I7
I8
I9/OE'
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
• Up to 16 inputs
• Up to 8 outputs
16V8B_PAL.pdf
Simple Mode Logic Diagram
INPUT LINES
OUTPUT LOGIC
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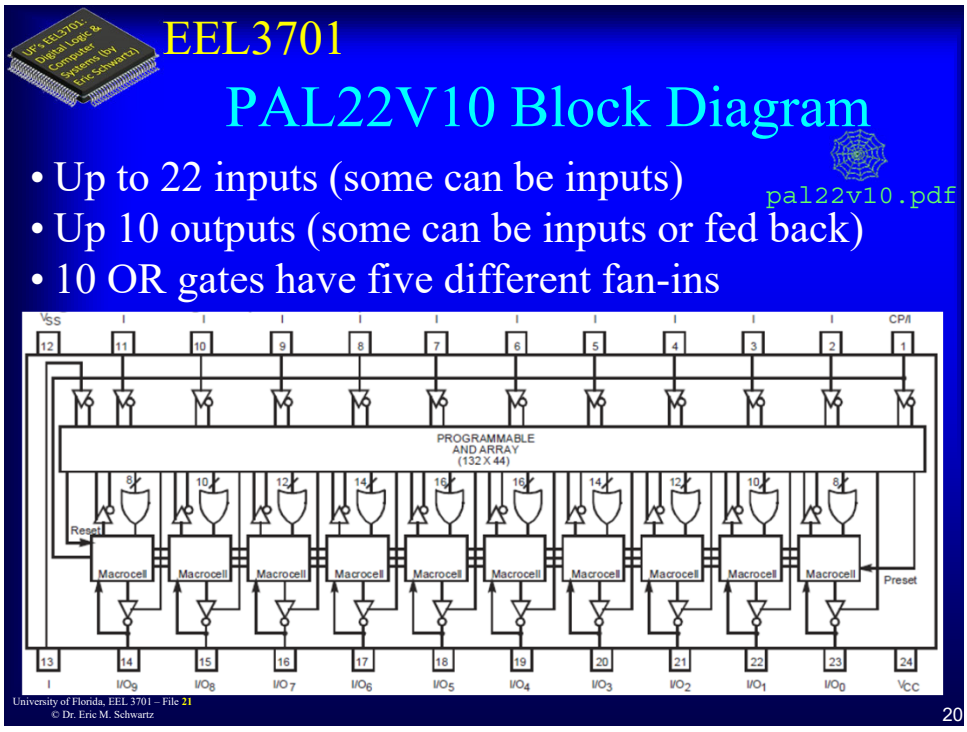
17


EEL3701
Output Logic Block: 16V8
Combinational Mode Option
XOR
16V8B_PAL.pdf
gal22v10.pdf
20
I0/CLK
VCC
GND
10
I1
16V8
I2
I3
I4
I5
I6
I7
I8
I9/OE'
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
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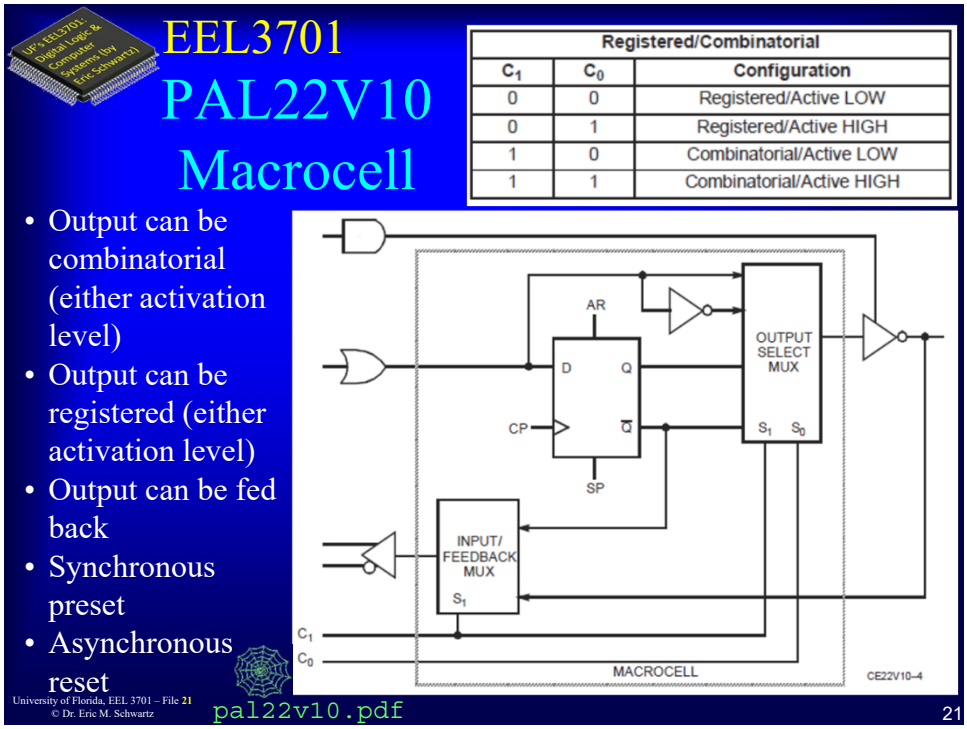
18


EEL3701 Output Logic Block: 16V8
Registered Mode Option
CLK
D
Q
XOR
OE
20
1
I0/CLK
VCC
GND
10
2
I1
16V8
3
I2
I/O0
12
4
I3
I/O1
13
5
I4
I/O2
14
6
I5
I/O3
15
7
I6
I/O4
16
8
I7
I/O5
17
9
I8
I/O6
18
11
I9/OE'
I/O7
19
• See also:
• PAL22V10
• GAL22V10
16V8B_PAL.pdf
pal22v10.pdf
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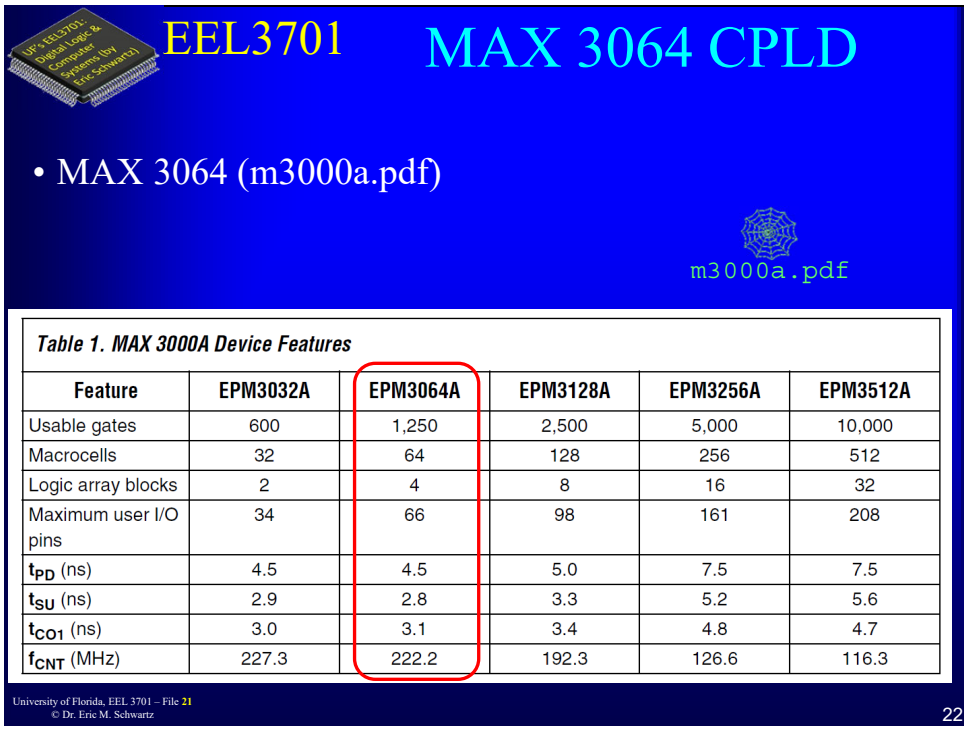
19


EEL3701
PAL22V10 Block Diagram
• Up to 22 inputs (some can be inputs)
• Up 10 outputs (some can be inputs or fed back)
• 10 OR gates have five different fan-ins
pal22v10.pdf
PROGRAMMABLE
AND ARRAY
(132 X 44)
Reset
Preset
Macrocell
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EEL3701
PAL22V10
Macrocell
Registered/Combinatorial
C1 C0 Configuration
0 0 Registered/Active LOW
0 1 Registered/Active HIGH
1 0 Combinatorial/Active LOW
1 1 Combinatorial/Active HIGH
• Output can be combinatorial (either activation level)
• Output can be registered (either activation level)
• Output can be fed back
• Synchronous preset
• Asynchronous reset
AR
D
Q
CP
SP
OUTPUT SELECT MUX
S1 S0
INPUT/ FEEDBACK MUX
S1
C1
C0
MACROCELL
CE22V10-4
pal22v10.pdf
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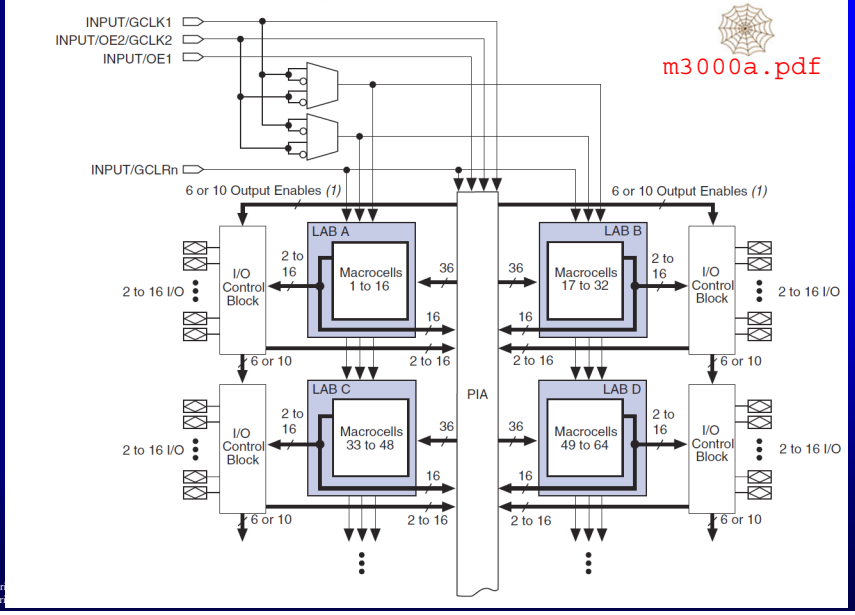
21


EEL3701
MAX 3064 CPLD
• MAX 3064 (m3000a.pdf)
m3000a.pdf
Table 1. MAX 3000A Device Features
Feature | EPM3032A | EPM3064A | EPM3128A | EPM3256A | EPM3512A
Usable gates | 600 | 1,250 | 2,500 | 5,000 | 10,000
Macrocells | 32 | 64 | 128 | 256 | 512
Logic array blocks | 2 | 4 | 8 | 16 | 32
Maximum user I/O pins | 34 | 66 | 98 | 161 | 208
tPD (ns) | 4.5 | 4.5 | 5.0 | 7.5 | 7.5
tSU (ns) | 2.9 | 2.8 | 3.3 | 5.2 | 5.6
tCO1 (ns) | 3.0 | 3.1 | 3.4 | 4.8 | 4.7
fCNT (MHz) | 227.3 | 222.2 | 192.3 | 126.6 | 116.3
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EEL3701 MAX 3064 CPLD

*Figure 1. MAX 3000A Device Block Diagram*

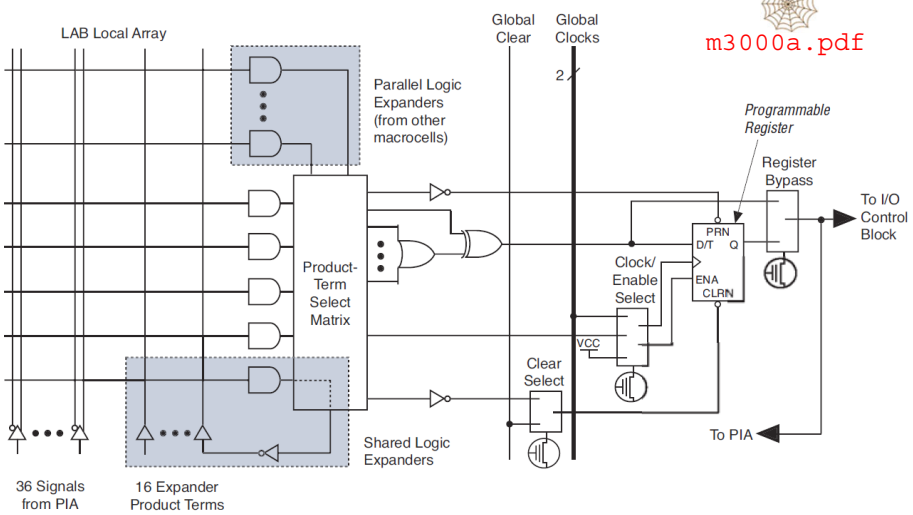



23

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EEL3701 MAX 3064 CPLD

*Figure 2. MAX 3000A Macrocell*



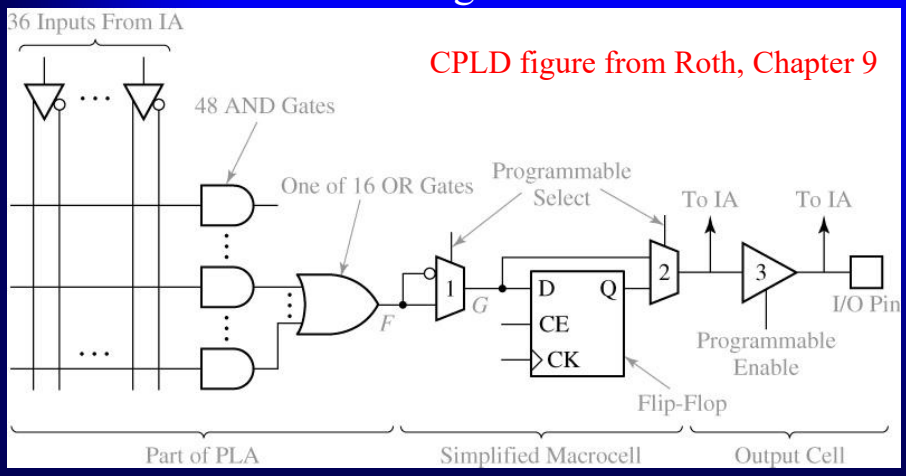

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EEL3701

## CPLD versus FPGA

- CPLD is a sum of products device, with multiple PLDs that do some sharing




CPLD figure from Roth, Chapter 9



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EEL3701

## CPLD versus FPGA

- CPLD is a sum of products device, with multiple PLDs that do some sharing

https://www.quora.com/What-is-the-difference-between-CPLD-and-FPGA

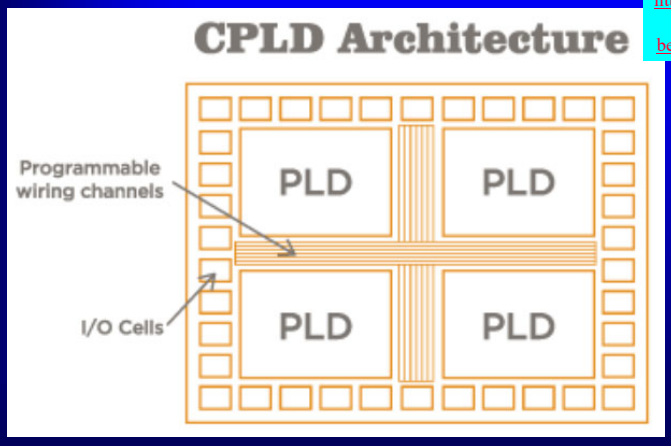
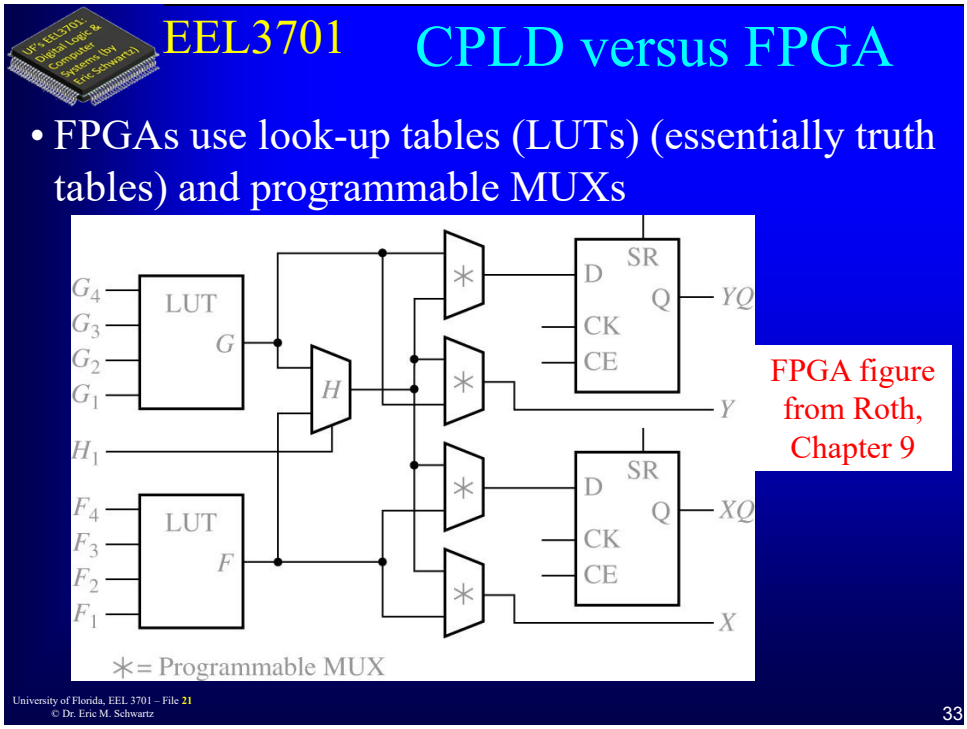


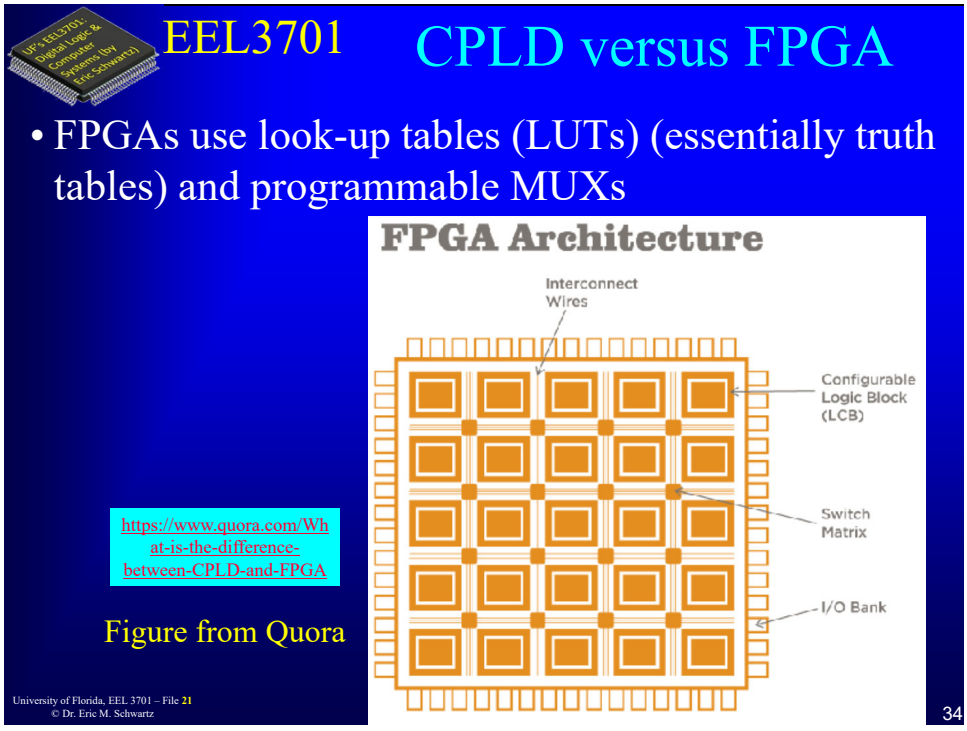

Figure from Quora



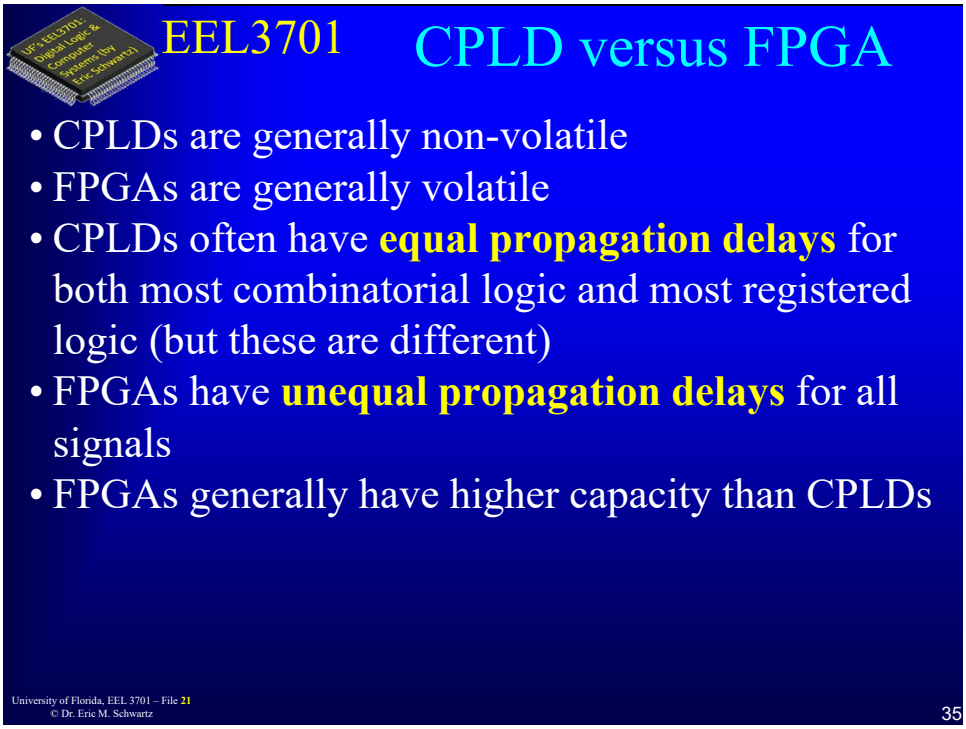
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EEL3701
CPLD versus FPGA
• FPGAs use look-up tables (LUTs) (essentially truth tables) and programmable MUXs
LUT
G
H
LUT
F
SR
D
Q
CK
CE
YQ
Y
XQ
X
= Programmable MUX
FPGA figure from Roth, Chapter 9
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EEL3701
CPLD versus FPGA
• FPGAs use look-up tables (LUTs) (essentially truth tables) and programmable MUXs
FPGA Architecture
Interconnect Wires
Configurable Logic Block (LCB)
Switch Matrix
I/O Bank
https://www.quora.com/What-is-the-difference-between-CPLD-and-FPGA
Figure from Quora
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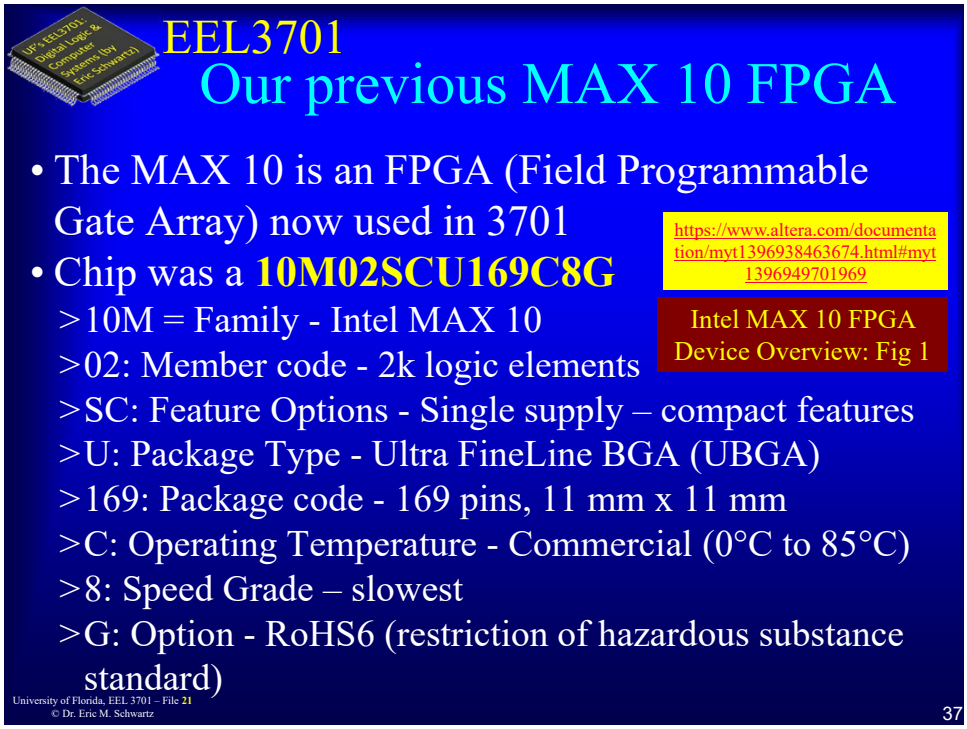
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EEL3701
CPLD versus FPGA
• CPLDs are generally non-volatile
• FPGAs are generally volatile
• CPLDs often have equal propagation delays for both most combinatorial logic and most registered logic (but these are different)
• FPGAs have unequal propagation delays for all signals
• FPGAs generally have higher capacity than CPLDs
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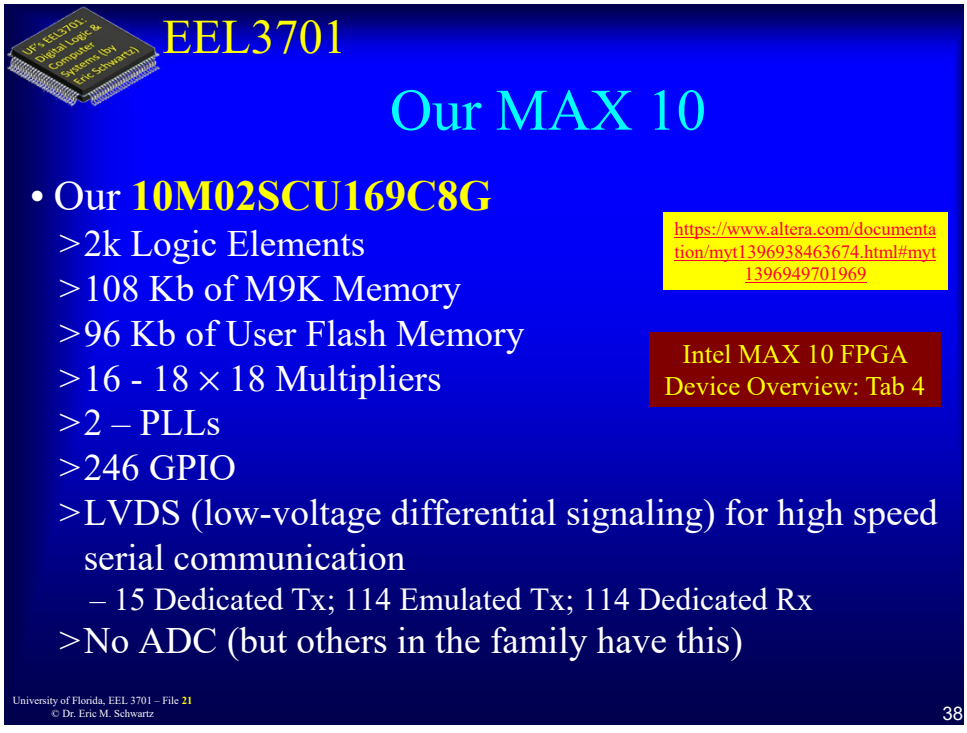
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EEL3701
MAX 10 FPGA on DE10-Lite
• The MAX 10 is an FPGA (Field Programmable Gate Array) now used in 3701
• Our chip is a 10M50DAF484C7G
>10M = Family - Intel MAX 10
>50: Member code - 50k logic elements
>DA: Feature Options – Dual supply (analog & flash)
>F: Package Type - FineLine BGA (FBGA)
>484: Package code - 484 pins, 23 mm x 23 mm
>C: Operating Temperature - Commercial (0°C to 80°C)
>7: Speed Grade – middle
>G: Option - RoHS6 (restriction of hazardous substance standard)
https://www.altera.com/documentation/myt1396938463674.html#myt1396949701969
Intel MAX 10 FPGA Device Overview: Fig 1
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EEL3701
Our previous MAX 10 FPGA
• The MAX 10 is an FPGA (Field Programmable Gate Array) now used in 3701
• Chip was a 10M02SCU169C8G
>10M = Family - Intel MAX 10
>02: Member code - 2k logic elements
>SC: Feature Options - Single supply – compact features
>U: Package Type - Ultra FineLine BGA (UBGA)
>169: Package code - 169 pins, 11 mm x 11 mm
>C: Operating Temperature - Commercial (0°C to 85°C)
>8: Speed Grade – slowest
>G: Option - RoHS6 (restriction of hazardous substance standard)
https://www.altera.com/documentation/myt1396938463674.html#myt1396949701969
Intel MAX 10 FPGA Device Overview: Fig 1
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Our MAX 10
• Our 10M02SCU169C8G
>2k Logic Elements
>108 Kb of M9K Memory
>96 Kb of User Flash Memory
>16 - 18 × 18 Multipliers
>2 – PLLs
>246 GPIO
>LVDS (low-voltage differential signaling) for high speed serial communication
– 15 Dedicated Tx; 114 Emulated Tx; 114 Dedicated Rx
>No ADC (but others in the family have this)
https://www.altera.com/documentation/myt1396938463674.html#myt1396949701969
Intel MAX 10 FPGA Device Overview: Tab 4
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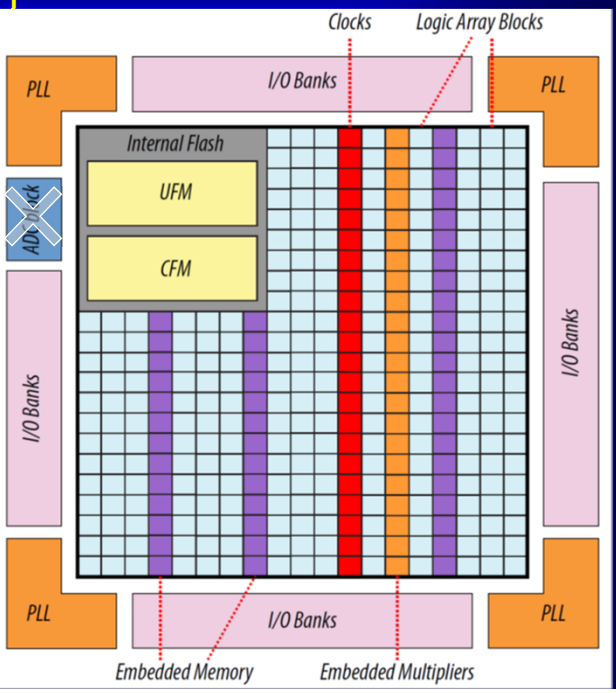
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# Max10 Floorplan

Max 10 Architecture: Fig 1

https://mil.ufl.edu/3701/docs/Max10/m10_architecture.pdf



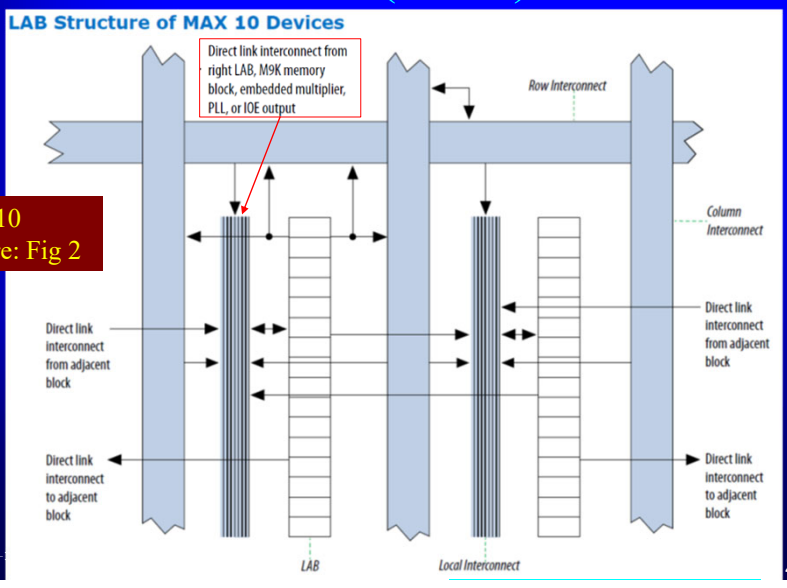



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# Max10 Logic Array Block (LAB) Structure

Max 10 Architecture: Fig 2

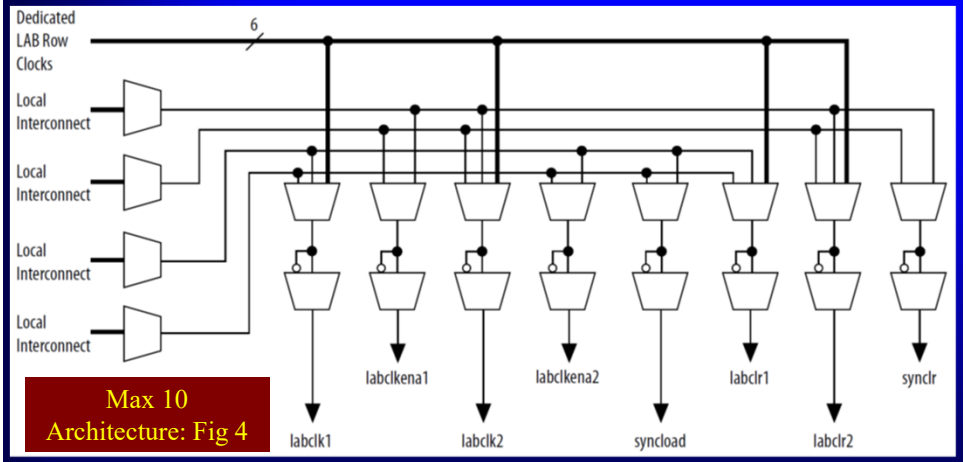





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# Max10 LAB-Wide Control Signals Structure




Max 10 Architecture: Fig 4

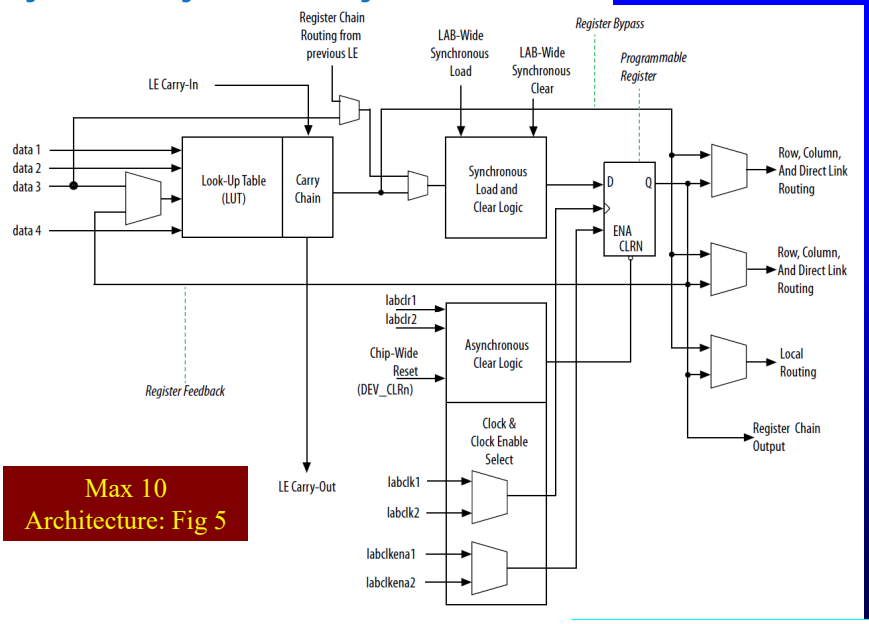


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# MAX 10 Architecture

**Figure 5. LE High-Level Block Diagram for MAX 10 Devices.**



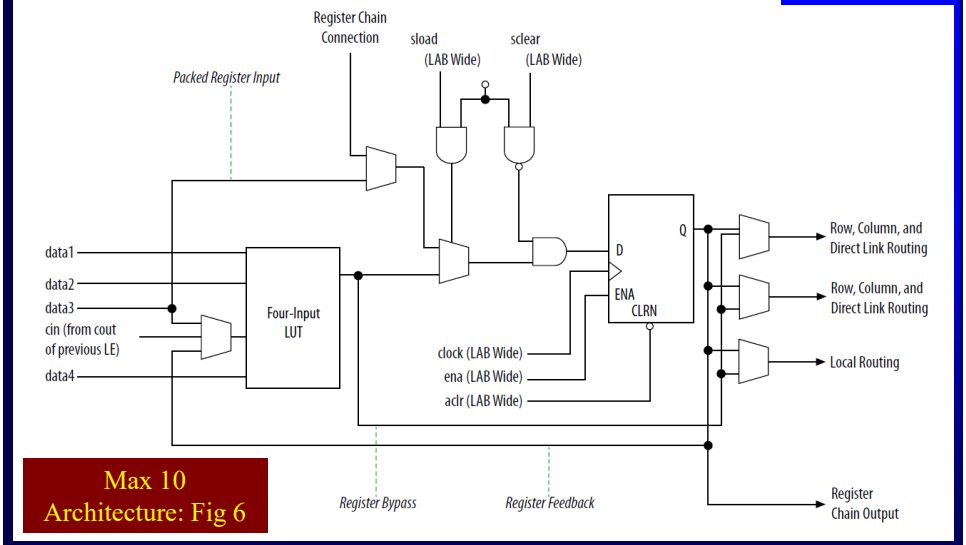

Max 10 Architecture: Fig 5

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EEL3701 MAX 10 Architecture

**Figure 6. LE Operating in Normal Mode for MAX 10 devices**

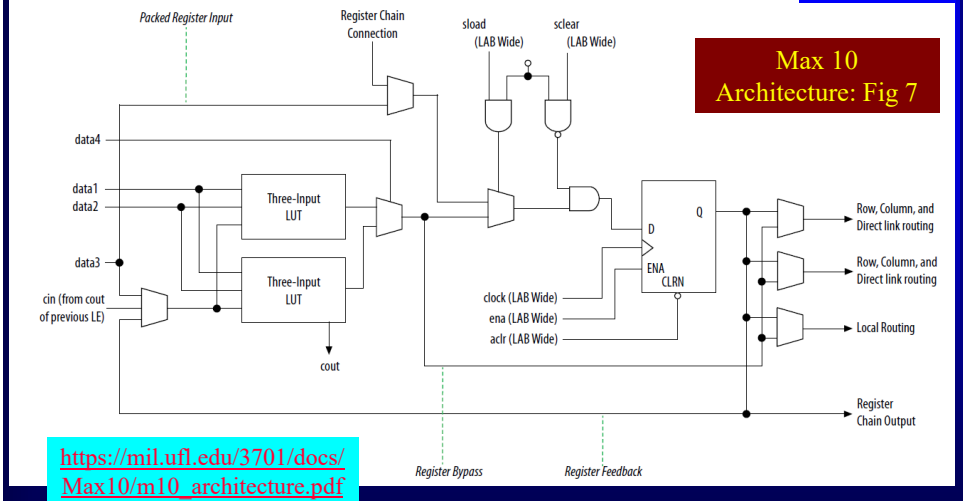



Max 10 Architecture: Fig 6



EEL3701 MAX 10 Architecture

**Figure 7. LE Operating in Arithmetic Mode for MAX 10 devices**




Max 10 Architecture: Fig 7

https://mil.ufl.edu/3701/docs/Max10/m10_architecture.pdf

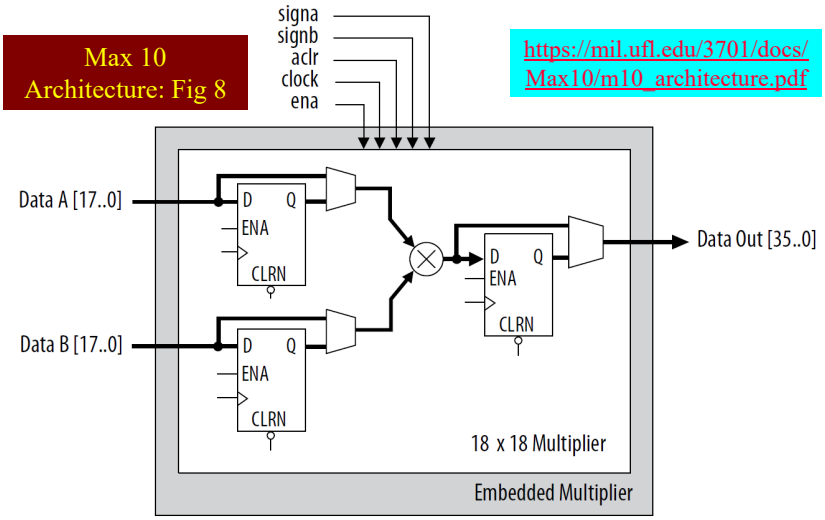
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## MAX 10 Architecture

**Figure 8. 18-Bit Multiplier Mode**

Max 10 Architecture: Fig 8

https://mil.ufl.edu/3701/docs/Max10/m10_architecture.pdf






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# *The End!*



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